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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,016	05/30/2001	Chaitanya Palusa	ALNC-9400	3233

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STALLMAN & POLLOCK LLP
SUITE 2200
353 SACRAMENTO STREET
SAN FRANCISCO, CA 94111

EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/873,016	PALUSA ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-14 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5 and 14* is/are rejected.

7)☒ Claim(s) *3,6-13 and 16-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 05/13/2005 has been entered. Claims 1, 3-14, and 16-20 are pending in this Office action.

Response to Arguments

2. Applicant's arguments with respect to claims 1 and 14 have been considered but are moot in view of the new ground(s) of rejection.

3. Claim objection has been withdrawn because claim number was missing in previous Office action.

Claim Objections

4. Claim 16 is objected to because of the following informalities: in line 3, "les" should be changed to -- less --. Appropriate correction is required.

5. Claim 4 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim should refer to other claims in the alternative only. See MPEP § 608.01(n). Accordingly, the claim 4 has not been further treated on the merits.

Comments: claim 4 is objected because claim depends on cancelled claim 2. However, if claim 4 depends on claim 1, claim 4 is a duplicate of claim 5 and would be objected for being a duplicate claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4-5, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaoka U.S. Patent 6,166,572 in view of Watanabe U.S. Patent 5,910,741 and Zhang et al. U.S. Patent 5,559,476.

Regarding claim 1, in column 4, lines 5-67, figure 1 illustrates a clock/data recovery apparatus including a PLL 10, which includes a voltage-controlled oscillator 104.

Yamaoka does not teach a voltage-controlled delay line (VCDL) as set forth in the claim. In column 1, lines 23-65, Zhang et al. discusses in figure 1 a voltage controlled oscillator (VCO) 20 including a plurality of current controlled delay cells, 25-1 to 25-k, connected together to form a k-stage ring oscillator, wherein an input of each current controlled delay cell (or stage) in the ring oscillator is connected to an output of another current controlled delay cell in the ring oscillator. Accordingly, the control voltage Vcnt applied to the gate of the n-

mos transistor 21 controls the period of oscillation of the VCO 20 by controlling the current flowing into each of the current controlled delay cells, 25-1 to 25-k, which in turn, controls the delay of each of the current controlled delay cells, 25-1 to 25-k, which in turn, determines the period of oscillation of the VCO 20. In light of that, the current controlled delay cells, 25-1 to 25-k correspond to the claimed limitations "*a fine delay stage having a number of devices ...*", the gate of the n-mos transistor 21 to which the control voltage Vcnt applied corresponds to the voltage-controlled current stage. The gate of the n-mos transistor 21 outputs a switching current Icnt having a magnitude defined by Vcnt to control the current flowing into each of the current controlled delay cells, 25-1 to 25-k. Zhang et al. and Yamaoka teachings are in the same field of endeavor. Because Zhang et al. further discusses the prior art VCO is particularly useful in phase-locked loop circuits such as PLL 100 in figure 2; see column 3, lines 35-40, therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention Yamaoka PLL can be modified to include the VCO as described by Zhang et al. in the prior art.

Referring back to Yamaoka invention, PLL 10 further includes a phase/frequency detector (PFD) 101, connected to the VCO for detecting a phase difference between a reference clock REFCLK and a delayed clock through DIV 105. In column 4, lines 35-50, the phase/frequency detector 101 asserting an "UP" signal when a reference clock signal leads the output delayed clock signal, and asserting an "DOWN" signal when a reference clock signal lags

the output delayed clock signal. The PFD 101 differs from the claimed phase detector in that the phase/frequency detector 202 asserting no synch signal when the reference clock signal and the output delayed clock signal are in phase. However, by not asserting the "UP" signal and the "DOWN" signal, the phase/frequency detector 202 implies a synch signal. Nevertheless, in column 4 lines 50-67, Watanabe shows a phase comparator 11 in a phase locked loop, wherein the phase comparator 11 generates an up-down signal when a reference clock signal RCLK is phase-advanced to an output clock signal CLK and vice versa, and *a phase lock signal HOLD* when phases of reference clock signal RCLK and output clock signal CLK are in phase. In light of Watanabe teachings, it would have been obvious for one of ordinary skill in the art at the time the invention was made that the phase/frequency detector 202 can be modified to assert a phase lock signal HOLD as taught by Watanabe. The motivation for combining the teachings is that physically asserting the phase-lock signal HOLD is evidently a selection at design. The PFD 101 as taught by Yamaoka still generates three states UP, DOWN, and without any signal for SYNCH, and performs the same function as the claimed phase detector.

The PLL 10 includes a charge pump 102 connected to the PFD 101 that outputs a pump voltage in response to the output signal from the PFD 101.

A low-pass filter 103 connected to charge pump 102 and the VCO that filters the pump voltage to output a control voltage.

An I clock/data recovery circuits 2-1 including (referring to FIG. 3) a voltage-controlled delay line 2-1-1 comprises fourteen voltage-control led NOR gates, numbered 2-1-111 to 2-1-119 and (2-1-1110 to 2-1-1114, and five AND gates 2-1-121 to 2-1-125. The voltage-controlled NOR gates in the voltage-controlled delay line 2-1-1 have the same configuration as the voltage-controlled NOR gates in the VCO 104 in the PLL 10, each comprising a NOR logic circuit and a delay control transistor (reference numerals omitted). The control voltage V obtained from the PLL 10 is applied to the gate electrodes of the delay control transistors in all of the voltage-controlled NOR gates 2-1-111 to 2-1-1114, and controls their propagation delays. In light of the foregoing, the voltage-controlled delay line 2-1-1 corresponds to the claimed delay circuit as set forth in the claim.

Regarding claim 4, for purpose of art rejection, claim 4 is also rejected. Referring to Watanabe invention, see figure 3, column 5 line 40 via column 6 line 55, FIG. 3 is a circuit diagram illustrating a circuit example of the phase comparator 13 according to the embodiment, including two flip-flops 16 and 17, three NAND gates 18 to 20, two inverters 21 and 22, three RS (Reset-Set type) latches 23 to 25 and an AND gate 26. flip-flops 16 and 17 correspond to the claimed "first rising edge detecting circuit" and "second rising edge detecting circuit". When the reference clock signal RCLK and the output clock signal CLK are synchronized with each other, the outputs NUP and NDN turn to LOW at the same time.

Regarding claim 5, claim is rejected on the same ground as for claim 4 because of similar scope.

Allowable Subject Matter

6. Claims 3, 6-13 and 16-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanhcong Tran 08/03/2005

Examiner KHANH TRAN